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**PATENT**

# IN THE U.S. PATENT AND TRADEMARK OFFICE

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| Appellants: | Ki-Myung YOON |
| Application No.: | **10/681,254** |
| Art Unit: | 2841 |
| Filed: | October 9, 2003 |
| Examiner: | Ivan H. Carpio |
| For: | MULTI-CHIP SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING THE SAME |
| Atty. Dkt. No.: | 2557-000171/US |
| Conf. No.: | 7505 |

October 19, 2007

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## APPELLANTS' BRIEF ON APPEAL UNDER 37 C.F.R. §41.37

Sir:

Appellants submit herewith their Brief on Appeal as required by 37 C.F.R. § 41.37.

| | **Claims remaining after Amendment** | | **Highest number previously paid for** | | **Present extra** |
|---|---|---|---|---|---|
| **Total** | 24 | - | 24 | = | 0 |
| **Independent** | 3 | - | 3 | = | 0 |

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## BRIEF ON BEHALF OF APPELLANTS

In support of the Notice of Appeal filed on March 19, 2007, appealing the Examiner's rejection made in the Office Action (hereinafter "Action") mailed on December 18, 2006 of each of pending claims 1-21 of the present application which appear in the attached (IX) Claims Appendix, Appellants hereby provide the following remarks.

## I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Samsung Electronics Co., Ltd., as evidenced by the Assignment recorded at Reel 014868 and Frame 0761.

## II. RELATED APPEALS AND INTERFERENCES

Appellants' legal representative is aware of no appeals or interferences that will affect, be directly affected by, or have a bearing on the Board of Patent Appeals and Interferences (hereinafter "the Board") decision in the pending Appeal.

## III. STATUS OF CLAIMS

Claims 1-24 are pending in the current application, with claims 1, 12 and 16 being written in independent form.

Appellants are appealing the twice rejection of claims 1-21. Claims 1-24, on appeal, are listed in the attached (IX) Claims Appendix.

## IV. STATUS OF AMENDMENTS

Appellants filed an Amendment under 37 C.F.R. §1.114 on August 17, 2006, which included amendments to claims 1 and 12 and newly-added claims 22-24. Appellants submit that the Amendment filed on August 17, 2006 has been entered and considered by the Examiner as evidenced on page 2 of the Action.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1 and 12 are directed to a multi-chip semiconductor package including (*inter alia*) (i) an enclosure body covering substantially the entire upper surface of the substrate and (ii) a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface.

Independent claim 16 is directed to a method of manufacturing a multi-chip semiconductor package including (*inter alia*) (i) forming an enclosure body encapsulating the upper surface of the substrate, the semiconductor chip and the conductive studs and (ii) removing an upper portion of the enclosure body to expose an upper surface of the conductive studs.

Referring to Fig. 2, example embodiments disclose a multi-chip semiconductor chip including an enclosure body (135) formed on the entire surface of the substrate (110) where the semiconductor chip (120) is mounted and a plurality of studs (130) are formed through the enclosure body on both sides of the semiconductor chip (120).[1] The studs (130) are used to provide electrical connections between the upper and lower packages in a multi-chip semiconductor package.[2] As illustrated in this embodiment, both the semiconductor chip (120) and the studs (130) may be mounted within the enclosure body (135), thereby reducing the misalignment margin relative to a conventional multi-chip semiconductor package.[3]

A solder ball (140) is installed in the insulating layer (105) corresponding to each of the studs (130) of the upper package structure (101a) for providing electrical connections to the studs (130) of the lower package structure (101b).[4] As illustrated in this exemplary embodiment, the enclosure body (135) is formed on the entire surface of the substrate (110) and the studs (130) are installed in a predetermined portion of the enclosure body (135).[5] Thus, the solder ball (140) need not have a height greater than that of the semiconductor chip (120) (or the enclosure body (135)) and the height of the multi-chip semiconductor package can be decreased accordingly.[6]

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[1] Specification, para. [0029].
[2] *Id.*
[3] *Id.*
[4] Specification, para. [0030].
[5] *Id.*
[6] *Id.*

Also, because the enclosure body (135) is formed on the entire surface of the substrate (110), the load is more evenly applied across the substrate (110) and the mechanical strength of the multi-chip semiconductor package can be improved or maintained while using a substrate having a reduced thickness.[7]

Referring to Fig. 3, other example embodiments disclose a multi-chip semiconductor package including an enclosure body (235) formed on the entire surface of the substrate (210) where the semiconductor chip (220) is recessed, and a plurality of studs (230) are disposed in predetermined portions of the enclosure body such as, for example, on both sides of the semiconductor chip.[8] The studs (230) are used as pads to provide electrical connection between the upper (201a) and lower (201b) packages in the multi-chip semiconductor package.[9]

Solder balls (240) provided in the insulating layer (205) corresponding to each of the studs (230) of the upper package (201a) are electrically connected to the corresponding studs (230) of the lower package structure (201b).[10] According to this exemplary embodiment, the recessed semiconductor chip (220) can produce a thinner overall semiconductor device and allow the use of a substrate having a reduced mechanical strength.[11]

Referring to Figs. 4 and 5, example embodiments disclose a multi-chip semiconductor package including an enclosure body (335) formed on the entire surface of the substrate (310) where the semiconductor chip (320) is mounted.[12] A plurality of studs (330) may be provided through predetermined portions of the enclosure body (335), for example, on both sides of the semiconductor chip (320).[13] The studs (330) are used as paths for electrically connecting the upper (301a) and lower (301b) packages in a multi-chip semiconductor package.[14]

Solder balls (340) installed in the insulating layer (305) and corresponding to each of the studs (330) in the upper package (301a) may be used to provide electrical connections to the corresponding studs (330) of the lower package structure (301b).[15]

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[7] Specification, para. [0031].
[8] Specification, para. [0035].
[9] *Id.*
[10] Specification, para. [0036].
[11] *Id.*
[12] Specification, para. [0038].
[13] *Id.*
[14] *Id.*
[15] Specification, para. [0039].

This embodiment may also be adapted to a ball-grid-array (BGA)-type multi-chip semiconductor package.[16] As illustrated in FIG. 5, the solder balls (340) of the upper package structure (301a) may be attached to the solder balls (340) of the lower package structure (301b), i.e., the insulating layers (305) of the substrates (310) may be attached facing each other to reduce the thickness of the resulting semiconductor devices.[17]

Referring to Fig. 6, other example embodiments disclose a multi-chip semiconductor package including an enclosure body (435) may then be formed on the entire surface of the substrate (410) where the semiconductor chip (420) is recessed.[18] Second studs (430) are provided through predetermined portions of the enclosure body (435), for example, on both sides of the semiconductor chip (420), and connected to the first conductive pattern (417).[19] A second conductive pattern (437) may then be formed in contact with the second stud (430).[20] The first and second conductive patterns, (417) and (437), may be formed with widths larger than the diameters of the first and the second studs, (415) and (430), and may be used as alignment subsidiary patterns.[21]

Meanwhile, a third conductive pattern (440) may be provided on the bottom of the conductive layer (405) of the substrate (410) corresponding to the first studs (415).[22] The third conductive pattern (440), in turn, is in electrical contact with the second conductive pattern of the lower package structure (401b).[23]

As described above, the substrate (410) may be formed from a stack of an insulating layer (400) of, for example a BT resin, and a conductive layer (405), with first and second studs (415) and (430) provided in the substrate (410) and the enclosure body (435), respectively.[24] Thus, the multi-chip semiconductor package according to this exemplary embodiment can be manufactured without requiring the use of solder balls having heights greater than the enclosure body (435).[25] Indeed, the first and second conductive patterns (417) and (437) may be used as an alternative to solder balls, thereby allowing the production of semiconductor devices having reduced thicknesses.[26]

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[16] Specification, para. [0040].
[17] *Id.*
[18] Specification, para. [0043].
[19] *Id.*
[20] *Id.*
[21] *Id.*
[22] Specification, para. [0044].
[23] *Id.*
[24] Specification, para. [0045].
[25] *Id.*
[26] *Id.*

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellants request the Board's review of the rejection of claims 1-24 under 35 U.S.C. §103(a) as being obvious over Londa, U.S. Patent No. 6,101,100 in view of Mostafazadeh et al. (hereinafter "Mostafazadeh"), U.S. Patent No. 5,783,870.

## VII. ARGUMENTS

### A. 35 U.S.C. §103(a) REJECTION – LONDA AND MOSTAFAZADEH

Appellants submit that claims 1-24 are allowable for features present in each claim. Appellants submit that the claims are argued in three groups. Group I includes claims 1-11, 21 and 22, which rise and fall together, with claim 1 being representative. Group II includes claims 12-15 and 23, which rise and fall together, with claim 12 being representative. Group III includes claims 16-20 and 24, which rise and fall together, with claim 16 being representative.

#### i GROUP I: CLAIMS 1-11, 21 AND 22

In view of the following arguments, Appellant submits that Londa in view of Mostafazadeh, as relied upon by the Examiner, fails to disclose or suggest a multi-chip semiconductor package including "an enclosure body covering substantially the entire upper surface of the substrate" and "a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface" as recited in independent claim 1.

### *a. Structural Differences between the Enclosure Body and Conductive Studs of the Present Application and the Cited Art*

Londa

The Examiner asserts that Londa discloses "...a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip (Fig. 2 elements 42, 44, 46)..."[27] Appellants respectfully disagree for the for the following reasons.

Appellants submit that the "enclosure body" and "conductive studs", recited in independent claim 1, fail to read upon the substrates 12, 22 and through holes 42/44/46, respectively, of Londa. That is, referring to Fig. 2 of Londa (reproduced below), Appellants submit that Londa explicitly teaches "...a plurality of plated through holes 42, 44, 46, 48, 50, 52 extending through first and second substrates 12, 22 and plane 30 for electrically coupling first and second layers of circuitry 20, 27."[28]

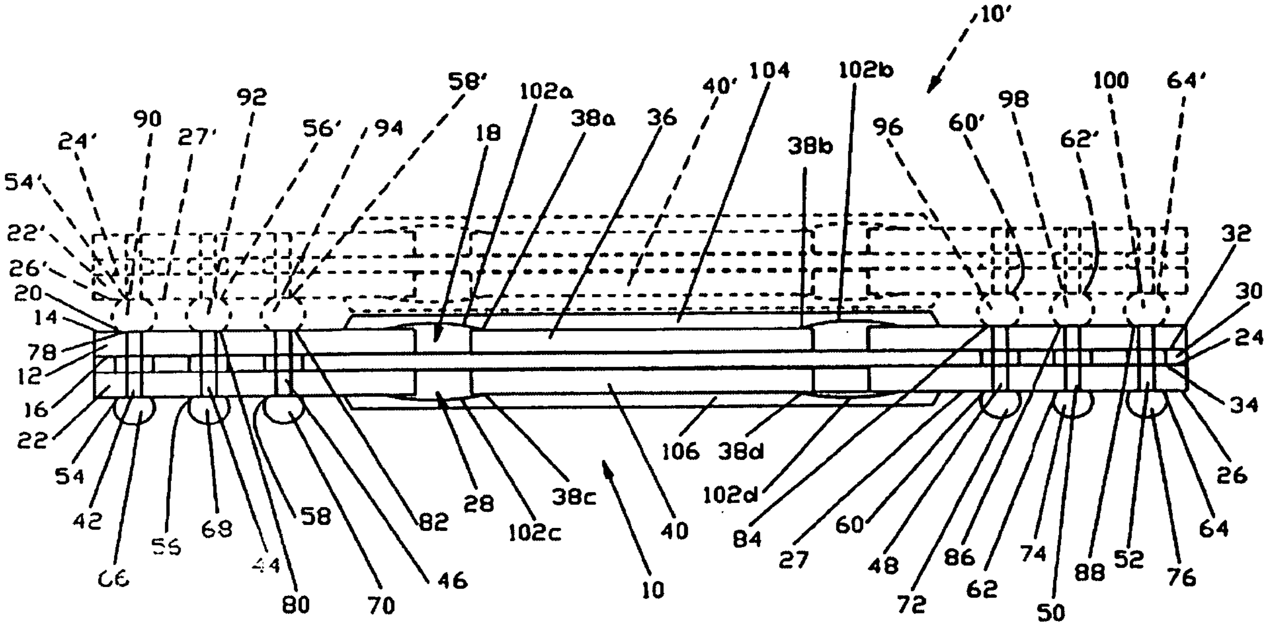

FIG. 2 OF LONDA

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[27] Action, p. 3.

[28] Londa, col. 4, ll. 15-29 (emphasis added).

That is, the through holes 42/44/46 are plated, not filled, with a conductive material. Thus, the through holes 42/44/46 are not "conductive studs" as recited in independent claim 1.

Furthermore, because the holes 42/44/46 of Londa (which extend through the first and second substrate 12/22) are coupled to the "circuitries" 20 and 27, the holes 42/44/46 are insulated from the electronic device 40' of the other package structure. Thus, the encapsulant 104 is spaced apart from the holes 42/44/46 by what is known as the misalignment margin. Accordingly, none of Londa's through-holes shown in Fig. 2 extend through any portion of the encapsulant.

Appellants further submit that the structure shown in Fig. 2 of Londa is merely conventional art as discussed in paragraphs [0005] – [0009] of the present application wherein a) the semiconductor devices 36,40 may be bonded to conductive pads or a pattern (not shown) of the substrates 12,22 by means of a wire 102, b) a plurality of through holes 42,44,46, which provide interlayer connecting paths, are formed through substrates 12,22 outside the periphery of the encapulsant 104, c) the plurality of through holes 42,44,46 are spaced from the encapulsant 104 by a predetermined distance in order to insulate them from the semiconductor chip 40' of the other package structure, and d) because the plurality of through holes 42,44,46 penetrate the substrate 12,22, the plurality of through holes 42,44,46 must be separated and insulated from the encapulsant 104.

Thus, if the plurality of through holes 42,44,46 extend through the substrate (as explicitly taught by Londa), the through holes 42,44,46 are spaced away from the encapsulant 104 in order to insulate the semiconductor chips 36 and 40 of package 10 from the semiconductor chip 40' of the package 10'.

Accordingly, Appellants submit that Londa fails to teach, or suggest, "a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface" as recited in independent claim 1.

### *Mostafazadeh*

Acknowledging the deficiency of Londa with respect to independent claim 1, the Examiner asserts that Mostafazadeh discloses "...a multi-chip having an enclosure body covering: substantially the entire upper surface of the substrate (Fig. 4a element 32). Londa and Mostafazadeh are analogous art because they are from the same field of endeavor (Multi-chip package). At the time [of] the invention, it would have been obvious to a person of ordinary skill in the art to modify the enclosure of Londa by having the enclosure covering the entire upper surface of the substrate. The suggestion or motivation for doing so would have been obvious in view of the teaching of Mostafazadeh, for providing protection (col. 6, lines 38-42)."[29] Appellants respectfully disagree with the Examiner for the following reasons.

Referring to Figs. 4A-4C (reproduced below), Appellants submit that Mostafazadeh's package does not include a substrate. Thus, Mostafazadeh fails to teach, or suggest, or "an enclosure body covering substantially the entire upper surface of the substrate" as recited in independent claim 1 and asserted by the Examiner.

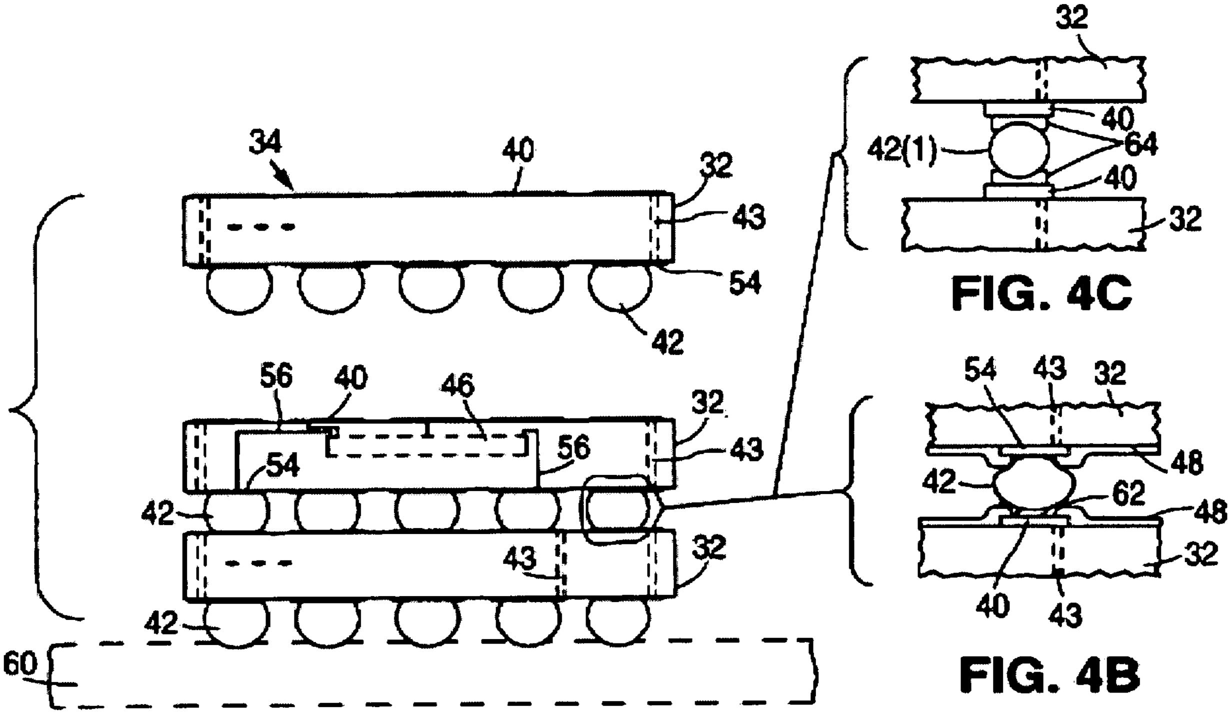

FIG. 4A

FIGS. 4A-4C OF MOSTAFAZADEH

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[29] Action, p. 3.

Mostafazadeh states "[a]n integrated circuit die 46 is also illustrated within package 32, where terminals of die 46 are connected, using wires, traces, and vias, to pads 40 and 54."[30] Because the die 46 is not connected to a substrate, insulation of the conductive via 43 from the die 46 is not necessary. Therefore, the die 46 may be formed within the package 32 (which the Examiner believes the enclosure body recited in independent claims 1 and 12 reads upon) and the conductive via 43 may extend through the package 32.

Accordingly, Appellants submit that Mostafazadeh fails to teach, or suggest, "an enclosure body covering substantially the entire upper surface of the substrate" as recited in independent claim 1. Thus, Mostafazadeh fails to remedy the deficiencies of Londa with respect to independent claim 1.

### *b. Improper Prima Facie Case of Obviousness: Combination of Cited Art Changes the Principle of Operation of the References*

Appellants submit that Mostafazadeh and Londa teach two different methods for electrically connecting the semiconductor devices wherein the methods that cannot be combined without changing the principle of operation of either reference. In particular, because the through-holes 42, 44, 46 of Londa extend through the substrate 12, 22, the package 32 of Mostafazadeh (wherein the conductive vias 43 extend through the package 32) may not be combine with the teaching of Londa such that the electronic devices 36, 40 of package 10 as taught by Londa would be insulated from the electronic device 40' of package 10'.

Appellants submit that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)..."[31] Accordingly, Appellants submit that the Examiner has not established a proper *prima facie* case of obviousness.

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[30] Mostafazadeh, col. 4, ll. 6-8 (emphasis added).

[31] MPEP §2143.01 (VI).

### c. *Lack of Motivation: Combination of the Cited Renders the References Unsatisfactory for Their Intended Purpose*

Furthermore, Appellants submit that Londa is directed to a multi-electronic device package that teaches stacking multiple electronic devices 36/40/40' in a single electronic package 10/10' in order to offer "higher chip density and less required interconnect density than two-dimensional multiple chip substrates."[32] Referring to Fig. 2 of Londa (reproduced above), Londa teaches "[f]irst encapsulant 104 may be bound to an encapsulant associated with second electronic package 10' to physically couple first electronic package 10 to the second electronic package 10'."[33] That is, contrary to the Examiner's assertion that "Londa teaches that [the] there is space between the encapsulants (see Fig. 2, the space between the adjacent encapsulants 104," Appellants submit that the encapsulant from the first package contacts the encapsulant from the second package and thus includes no separation between the encapsulated portions of the packages.[34] Thus, Londa's multi-electronic device package is directed to a device for reducing the package area.

Mostafazadeh is directed to a method for connecting packages of a stacked ball grid array structure wherein "[a]n air gap is formed between adjacent, stacked packages for cooling."[35] Thus, the stacked packages of Mostafazadeh are deliberately separated to allow for adequate ventilation. See Figure 5 of Mostafazadeh (reproduced below).

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[32] Londa, col. 1, ll. 3-5.

[33] Londa, col. 4, ll. 63-66.

[34] Office communication, March 17, 2006, p. 2.

[35] Mostafazadeh, Abstract.

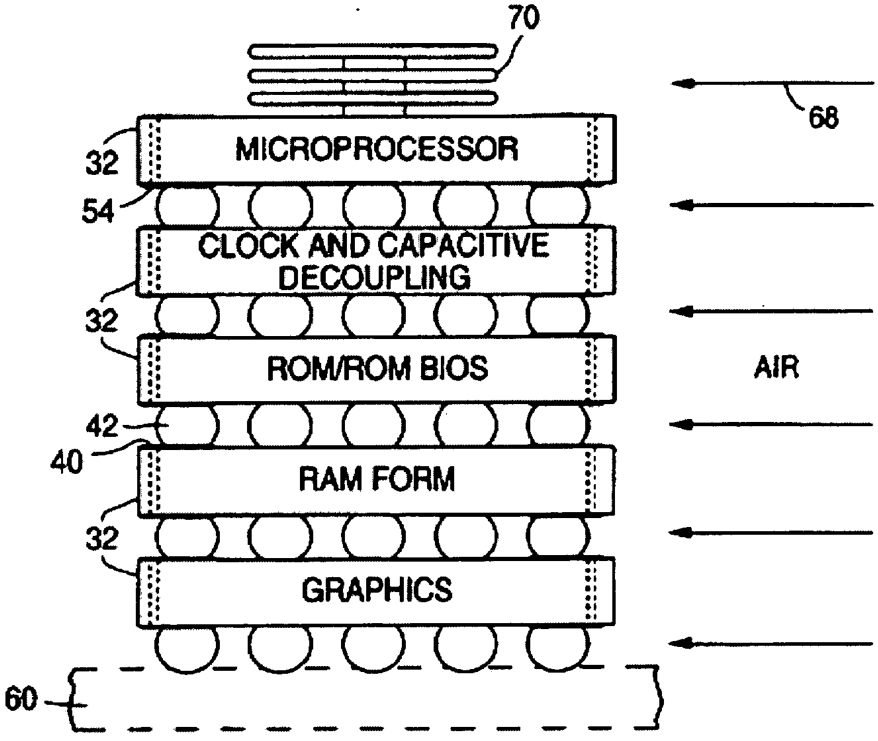

**FIG. 5 OF MOSTAFAZADEH**

Accordingly, assuming *arguendo* that one was motivated to position Londa's electronic device 36 in Mostafazadeh's enclosure body 32 such that the enclosure body covers "substantially the entire upper surface of the substrate" as recited in independent claim 1, Appellants submit that the enclosure body (having the solder balls thereon as taught by Mostafazadeh) would increase the space between the packages of Londa, and thus, increase the total area of the stacked package (contrary to the teachings of Londa).

Further assuming that one was motivated to form the enclosure body such that enclosure body of the first package contacts the enclosure body of second package (in order to reduce the total area of the stacked package as taught by Londa), Appellants submit that the enclosure bodies would block the flow of air between the packages in a manner contrary to the teachings of Mostafazadeh.

Appellants submit that "[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue."[36]

Appellants further submit that the combination of Londa and Mostafazadeh cannot be combined without rendering either reference unsatisfactory for its intended purpose. Moreover, "[i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)..."[37]

Accordingly, Appellants maintain that there is no motivation to combine Londa and Mostafazadeh.

### ii. GROUP II: CLAIMS 12-15 AND 23

Claim 12 recites a multi-chip semiconductor package including "an enclosure body covering substantially the entire upper surface of the substrate" and "a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface."

Appellants submit that claim 12 is allowable over Londa at least for similar reasons as given above with respect to independent claim 1. In addition, Mostafazadeh fails to remedy the deficiencies of Londa with respect to independent claim 12. Thus, Londa in view of Mostafazadeh also fails to disclose or suggest the all of the features recited in claim 12.

### iii. GROUP III: CLAIMS 16-20 AND 24

Claim 16 recites a method of manufacturing a multi-chip semiconductor package including "forming an enclosure body encapsulating the upper surface of the substrate, the semiconductor chip and the conductive studs" and "removing an upper portion of the enclosure body to expose an upper surface of the conductive studs."

Appellants submit that claim 16 is allowable over Londa at least for similar reasons as given above with respect to independent claim 1. In addition, Mostafazadeh fails to remedy the deficiencies of Londa with respect to independent claim 16. Thus, Londa in view of Mostafazadeh also fails to disclose or suggest the all of the features recited in claim 16.

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[36] *KSR Int'l Co.* v. *Teleflex Inc.*, (U.S. Apr. 30, 2007) (No. 04-1350) (emphasis added).
[37] MPEP §2143.01(V).

## VIII. CONCLUSION

Appellants respectfully request the Board to reverse the Examiner's obviousness rejection of claims 1-24.

The Commissioner is authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By:____________________________
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JAC/CDW

Attachments: IX. Claims Appendix
IIX. Evidence Appendix
IIIX. Related Proceeding Appendix

## IX. CLAIMS APPENDIX

1. A multi-chip semiconductor package comprising:

a plurality of stacked semiconductor package structures, each semiconductor package structure including;

a substrate having an upper surface and a lower surface;

a semiconductor chip mounted on the upper surface of the substrate, the semiconductor chip including an active surface and a backside surface;

an enclosure body covering substantially the entire upper surface of the substrate;

a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface; and

at least one conductive member formed in contact with the lower surface of at least one of the conductive studs.

2. A multi-chip semiconductor package according to claim 1, wherein:

the stacked semiconductor package structures include an upper package structure and a lower package structure, the upper package structure and the lower package structure having substantially the same configuration;

wherein the at least one conductive member of the upper package structure is in electrical contact with at least one conductive stud of the lower package structure.

3. A multi-chip semiconductor package according to claim 1, wherein:

the stacked semiconductor package structures include an upper package structure and a lower package structure, the upper package structure and the lower package structure having substantially the same configuration;

wherein the at least one conductive member of the upper package structure is in direct electrical contact with the at least one conductive member of the lower package structure.

4. A multi-chip semiconductor package according to claim 1, wherein:

the substrate includes

a conductive layer, the conductive layer having an upper surface and a lower surface, and

an insulating layer, the insulating layer being formed on the lower surface on the conductive layer.

5. A multi-chip semiconductor package according to claim 4, wherein:

the active surface of the semiconductor chip includes conductive pads, the conductive pads being electrically connected to the conductive layer.

6. A multi-chip semiconductor package according to claim 5, wherein:

backside surface of the semiconductor chip is recessed below a plane defined by the upper surface of the conductive layer.

7. A multi-chip semiconductor package according to claim 6, wherein:

the active surface of the semiconductor chip is substantially coplanar with or recessed below the plane defined by the upper surface of the conductive layer.

8. A multi-chip semiconductor package according to claim 5, wherein:

conductive balls are formed on a plurality of bond pads on the active surface of each semiconductor chip, the conductive balls providing direct electrical contact to the conductive layer.

9. A multi-chip semiconductor package according to claim 1, wherein:

the at least one conductive member includes a plurality of solder balls.

10. A multi-chip semiconductor package according to claim 1, wherein:

the at least one conductive member includes a conductive pattern.

11. A multi-chip semiconductor package according to claim 1, wherein:

the substrate includes conductive layer, the conductive layer having an upper surface and a lower surface, and an insulating layer formed on the upper surface of the conductive layer;

and further wherein

a second plurality of conductive studs extend through the insulating layer and are electrically connected to corresponding ones of the plurality of conductive studs extending through the enclosure body.

12. A multi-chip semiconductor package comprising:

an upper semiconductor package structure and a lower semiconductor package structure, each semiconductor package structure including;

a substrate having an upper surface and a lower surface and including a conductive layer and an insulating layer;

a semiconductor chip mounted on the upper surface of the substrate, the semiconductor chip including an active surface and a backside surface;

an enclosure body covering substantially the entire upper surface of the substrate;

a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip, the conductive studs having an upper surface and a lower surface;

wherein at least one conductive member is formed in contact with the lower surface of at least one of the conductive studs of the upper semiconductor package structure; and

the upper semiconductor package structure and the lower semiconductor package structure are positioned so that the at least one conductive member is in electrical contact with the upper surface of at least one conductive stud of the lower semiconductor package structure.

13. A multi-chip semiconductor package according to claim 12, wherein:

the at least one conductive member includes a plurality of solder balls formed on the lower surfaces of a plurality of the conductive studs of the upper semiconductor package structure; and

the plurality of solder balls are in electrical contact with the upper surfaces of corresponding conductive studs of the lower semiconductor package structure.

14. A multi-chip semiconductor package according to claim 12, wherein:

the semiconductor chip is mounted in a recessed orientation in which the backside surface lies below a plane defined by the upper surface of the substrate.

15. A multi-chip semiconductor package according to claim 12, wherein:

the insulating layer includes a resin material and the conductive layer includes a metallic material.

16. A method of manufacturing a multi-chip semiconductor package comprising:

providing a substrate, the substrate having an upper surface and a lower surface;

forming a plurality of conductive studs, the conductive studs extending through the substrate;

mounting a semiconductor chip on the upper surface of the substrate;

forming an enclosure body encapsulating the upper surface of the substrate, the semiconductor chip and the conductive studs;

removing an upper portion of the enclosure body to expose an upper surface of the conductive studs;

forming a conductive member on a portion of the lower surface of the substrate in electrical contact with the conductive studs to complete a semiconductor package structure; and

mounting a plurality of stacked semiconductor package structures so that the conductive member of an upper semiconductor package structure is in electrical contact with a lower semiconductor package structure.

17. A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein:

the conductive member of the upper semiconductor package structure is in electrical contact with conductive studs of the lower semiconductor package structure.

18. A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein:

the conductive member of the upper semiconductor package structure is in electrical contact with conductive member of the lower semiconductor package structure.

19. A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein:

providing the substrate includes:

forming conductive layer, the conductive layer having an upper surface and a lower surface;

forming an insulating layer on the lower surface of the insulating layer; and

removing portions of the insulating layer, the removed portions corresponding to locations of the conductive studs.

20. A method of manufacturing a multi-chip semiconductor package according to claim 19, wherein:

the insulating layer is a resin layer; and

the portions of the insulating layer are removed after forming the conductive studs.

21. A method of manufacturing a multi-chip semiconductor package according to claim 1 comprising:

forming the plurality of semiconductor package structures, each semiconductor package structure being formed by

preparing the substrate;

forming the plurality of conductive studs on the substrate, the conductive studs extending through the substrate;

mounting the semiconductor chip on the substrate;

forming electrical connections between the active surface of the semiconductor chip and the upper surface of the substrate on which the semiconductor chip is mounted;

forming the enclosure body encapsulating the upper surface of the substrate, the semiconductor chip, the electrical connections and the conductive studs;

removing an upper portion of the enclosure body to expose the upper surface of the conductive studs; and forming the conductive member on the lower surface of the substrate, the conductive member being in electrical contact with the lower surface of at least one of the conductive studs; and

stacking an upper semiconductor package structure and a lower semiconductor package structure whereby the conductive member of the upper semiconductor package structure is in electrical contact with a corresponding conductive stud on the lower semiconductor package structure.

22. A multi-chip semiconductor package according to claim 1, wherein the upper surface of the conductive studs extends to an upper surface of the enclosure body and the lower surface of the conductive studs extends to a lower surface of the enclosure body.

23. A multi-chip semiconductor package according to claim 12, wherein the upper surface of the conductive studs extends to an upper surface of the enclosure body and the lower surface of the conductive studs extends to a lower surface of the enclosure body.

24. A method of manufacturing a multi-chip semiconductor package according to claim 16, wherein forming the plurality of conductive studs includes:

extending an upper surface of the conductive studs to an upper surface of the enclosure body; and

extending a lower surface of the conductive studs to a lower surface of the enclosure body.

## IIX. EVIDENCE APPENDIX

NONE

## IIIX. RELATED PROCEEDINGS APPENDIX

NONE